Low Power Consumption exemplified using XOR Gate via different logic styles

Harshita Mittal, Shubham Budhiraja

Abstract- Performance being no more synonymous with only circuit speed and processing power but also power consumption, Low power has emerged as a principal theme in today's world of electronics industries. So, to design a low power VLSI circuit, non clocked styles like DCVSL & MDCVSL are being used. This paper is intended to show the most power efficient logic style for VLSI design for a particular circuit. It represents the simulation of different XOR Structures and their comparative analysis on different parameters such as power, supply voltage and temperature using DCVSL, MDCVSL & CMOS design methodologies. All the simulations have been carried out on Tanner Tools v13.0.

Index Terms - CMOS, DCVSL, MDCVSL, POWER EFFICIENT TECHNIQUE, TANNER TOOL, VLSI, XOR

1 INTRODUCTION

LOW power VLSI (Very Large Scale integrated Circuits) circuits have become an important criteria for designing energy efficient electronic designs for high performance and portable devices. As we know, VLSI Designing is an amalgamation of several processes; the simplest flow of VLSI design is as shown in Fig1.2.

In recent years, a wide variety of techniques have been developed to address the various aspects of the power problem and to meet ever more aggressive power specifications at each level. For example: at the chip design level, the new techniques include power shut-off (PSO), multi-supply multi-voltage (MSMV) etc, evolving from older techniques like clock gating [1]. In this work, we are primarily concerned about power efficient techniques at the circuit design level. This paper compares XOR structures made by different logic styles, on the basis of the power dissipation, supply voltage and the temperature dependence of the circuit.

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Figure 1.1. Logic diagram of XOR gate along with its truth table [2]

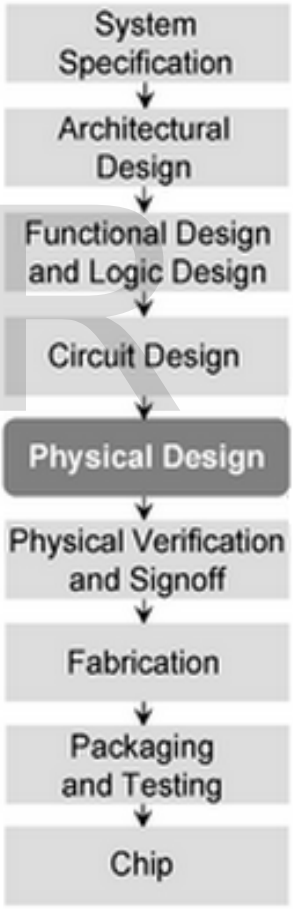

Fig 1.2. VLSI design flow [3]

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2. Sources For Power Dissipation

There are three major sources of power dissipation in CMOS circuits given by the following equation:

$$P_{total} = \alpha C_L V_{dd}^2 f_{clk} + I_{sc} V_{dd} + I_{leakage} V_{dd} \quad [4]$$

The first term represents the switching power where alpha is the switching factor, C is the loading capacitance, f represents the clock frequency and Vdd is the supply voltage. The second term is called short circuit power due to the direct path short circuit current, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. The last term represents the static power due to the leakage current, is primarily determined by fabrication technology considerations. The dominant term in a "well-designed" circuit is the switching component, and low power design thus becomes the task of minimizing the same while retaining the required functionality.

The requirements for low-power circuit implementation are as follows:

1. Load Capacitance reduction: This can be minimized by reducing the transistor count. However, extra transistors may be required to insure that charge sharing does not result in incorrect evaluation [4].

2. Supply voltage reduction: A logic style providing fast logic gates to speed up critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. So a logic style must be robust against supply voltage reduction [4].

3. Switching activity reduction: At the circuit level, large differences are primarily observed between static and dynamic logic styles. Only minor transition activity variations are observed among different static logic styles [4].

4. Short circuit current reduction: Short circuit currents (also known as dynamic leakage currents) may vary by a considerable amount between different logic styles. Their contribution to the overall power consumption is rather limited but not negligible (10-30 %), except for very low voltages where the short circuit currents disappear. A low-power design should have minimal short circuit current [4].

So, it can be condensed from the above study that we want a non clocked logic style having lower power consumption at any supply voltage and temperature.

3. Review Of Different XOR Structures

3.1 CMOS XOR Structure

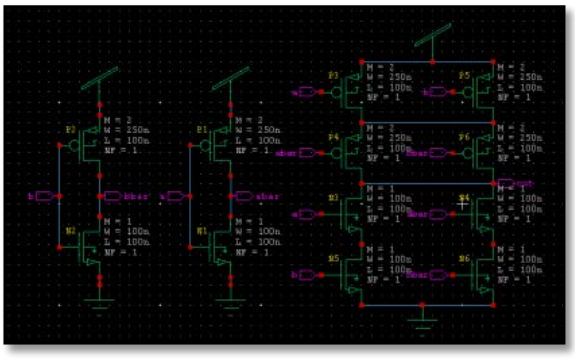

Fig 3.1.1. Schematic Diagram of XOR CMOS structure [6].

The Complementary MOSFET structure comprises of PMOS and NMOS, having inputs applied to the gate terminals of both the MOSFETS. Advantages of using CMOS logic: static power dissipation, ratio less design, noise margin. Disadvantages of using CMOS logic: area, complexity, capacitive loading, propagation delay [5].

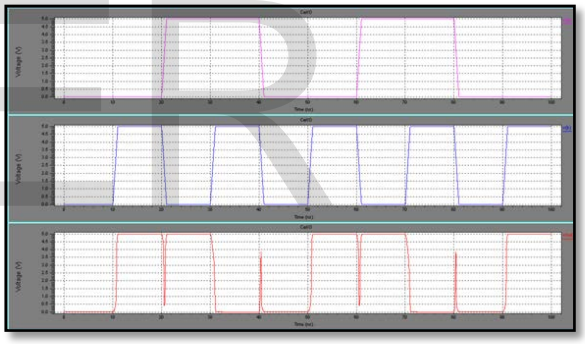

Fig 3.1.2. Output waveforms of XOR CMOS structure [6].

3.2 DCVSL XOR Structure

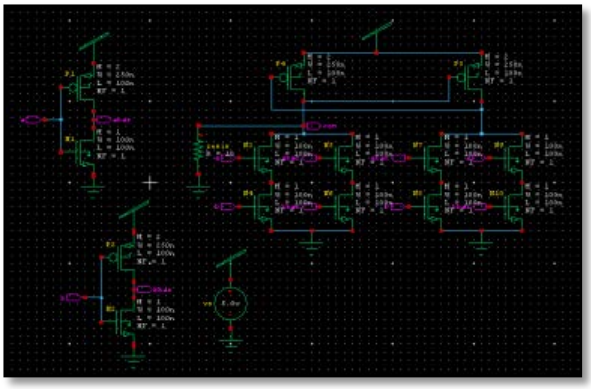

Fig 3.2.1. Schematic Diagram of XOR DCVSL structure [6].

In Differential Cascade Voltage Switch Logic, both the pull down networks will accept complementary inputs with respect

to each other and provide complementary outputs with respect to each other i.e. they are mutually exclusive networks. DCVSL provides rail to rail swing, high reliability and noise immunity. The limitations of using DCVSL are increased design complexity and doubled no of wires [5].

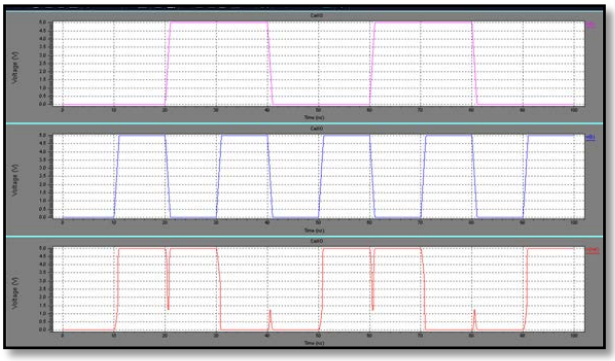

Fig 3.2.2. Output waveforms of XOR DCVSL structure [6].

3.3 MDCVSL XOR Structure

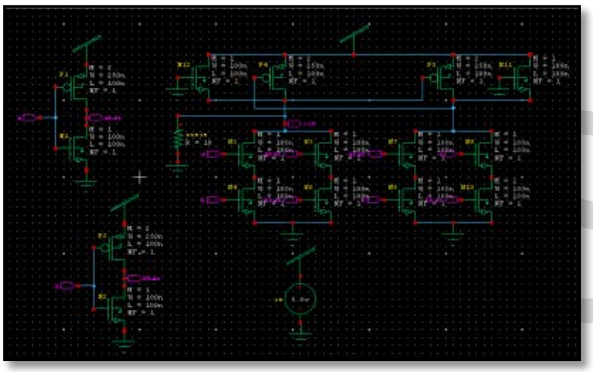

Fig 3.3.1. Schematic Diagram of XOR MDCVSL structure [6].

MDCVSL stands for modified differential cascade voltage switch logic. If we modify DCVSL circuit by adding two NMOS in parallel to the two PMOS, we get MDCVSL [7].

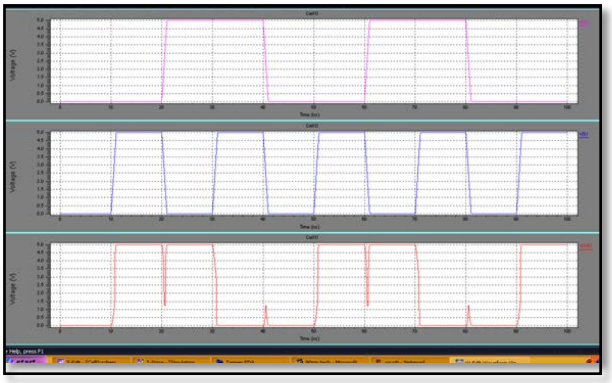

Fig 3.3.2. Output waveforms of XOR MDCVSL structure [6].

4. Simulation And Comparison

4.1 Plot of power consumption with supply voltage

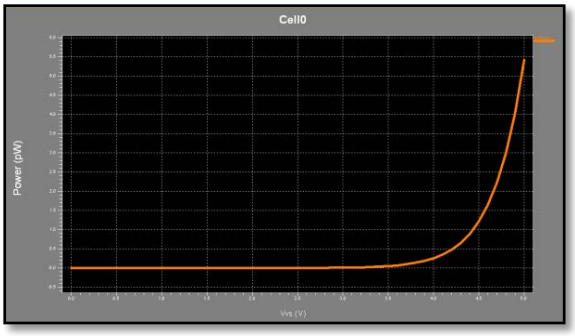

Fig 4.1.1. Waveform of XOR CMOS structure [6].

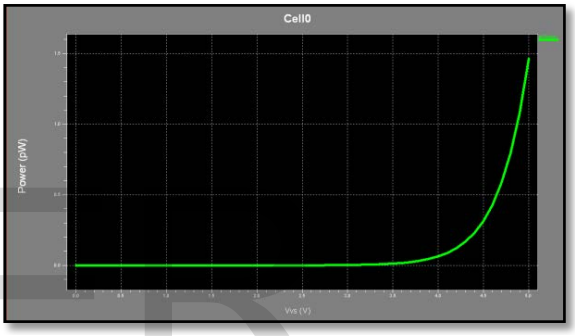

Fig 4.1.2. Waveform of XOR DCVSL structure [6].

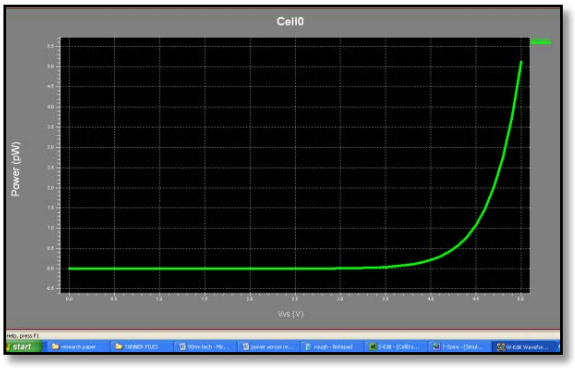

Fig 4.1.3. Waveform of XOR MDCVSL structure [6].

4.2 Plot of power consumption with temperature

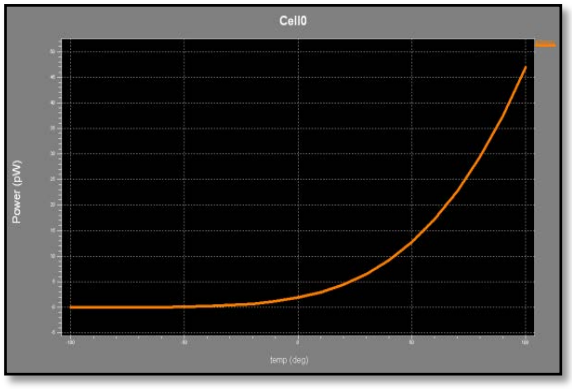

Fig 4.2.1. Waveform of XOR CMOS structure [6].

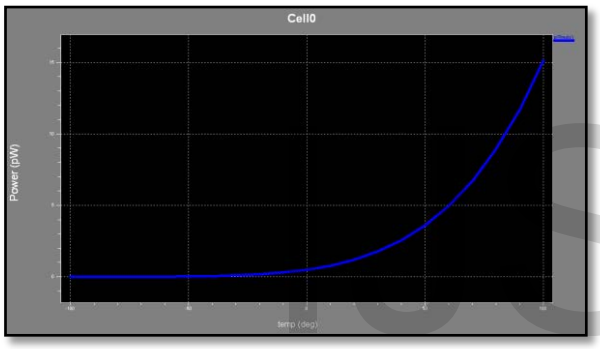

Fig 4.2.2. Waveform of XOR DCVSL structure [6].

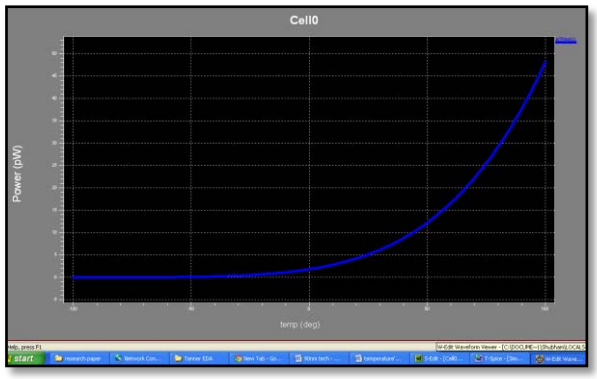

Fig 4.2.3. Waveform of XOR MDCVSL structure [6].

TABLE 1
PLOT OF POWER WITH TEMPERATURE

Temperature	MDCVSL	DCVSL	CMOS
-100	6.829e-016	1.8994e-016	7.5921e-016
-90	2.3489e-015	6.4029e-016	2.5577e-015
-80	7.017e-015	1.8863e-015	7.5273e-015
-70	1.8572e-014	4.9508e-015	1.9726e-014
-60	4.429e-014	1.1766e-014	4.6777e-014
-50	9.6551e-014	2.5666e-014	1.0173e-013
-40	1.9478e-013	5.1988e-014	2.0522e-013
-30	3.675e-013	9.8746e-014	3.8775e-013
-20	6.5428e-013	1.7734e-013	6.9174e-013
-10	1.1076e-012	3.033e-013	1.1733e-012
0	1.7945e-012	4.9694e-013	1.9034e-012
10	2.7977e-012	7.8402e-013	2.9677e-012
20	4.2166e-012	1.1963e-012	4.4666e-012
30	6.168e-012	1.7722e-012	6.5127e-012
40	8.7857e-012	2.5568e-012	9.2292e-012
50	1.2221e-011	3.6025e-012	1.2746e-011
60	1.6642e-011	4.9694e-012	1.7196e-011
70	2.2234e-011	6.7251e-012	2.2713e-011
80	2.9194e-011	8.9452e-012	2.9424e-011
90	3.7739e-011	1.1713e-011	3.7449e-011
100	4.8096e-011	1.5121e-011	4.6899e-011

TABLE 2
PLOT OF POWER WITH VVS (SUPPLY VOLTAGE)

Vvs (V)	MDCVSL	DCVSL	CMOS
0	0	0	0
0.1	1.1169e-019	5.3626e-020	1.8151e-019
0.2	1.6331e-019	7.5547e-020	2.9819e-019
0.3	2.4342e-019	1.1116e-019	4.4399e-019
0.4	3.6206e-019	1.6355e-019	6.5397e-019
0.5	5.3704e-019	2.4e-019	9.5985e-019
0.6	7.9499e-019	3.5149e-019	1.4058e-018
0.7	1.175e-018	5.1393e-019	2.0555e-018
0.8	1.7341e-018	7.5033e-019	3.0009e-018
0.9	2.5562e-018	1.094e-018	4.3753e-018
1	3.7633e-018	1.593e-018	6.371e-018
1.1	5.5342e-018	2.3167e-018	9.2656e-018
1.2	8.1294e-018	3.3653e-018	1.3459e-017
1.3	1.1928e-017	4.8826e-018	1.9527e-017
1.4	1.7483e-017	7.0756e-018	2.8296e-017
1.5	2.5595e-017	1.0241e-017	4.0955e-017
1.6	3.7428e-017	1.4805e-017	5.9204e-017
1.7	5.4668e-017	2.1377e-017	8.5477e-017
1.8	7.9751e-017	3.0826e-017	1.2325e-016
1.9	1.162e-016	4.4393e-017	1.7749e-016
2	1.6908e-016	6.3846e-017	2.5524e-016
2.1	2.457e-016	9.1697e-017	3.6654e-016
2.2	3.5653e-016	1.3151e-016	5.2561e-016
2.3	5.166e-016	1.8832e-016	7.5259e-016
2.4	7.4738e-016	2.6928e-016	1.0759e-015
2.5	1.0795e-015	3.8442e-016	1.5356e-015
2.6	1.5567e-015	5.4789e-016	2.1881e-015
2.7	2.241e-015	7.7956e-016	3.1124e-015
2.8	3.2201e-015	1.1073e-015	4.4191e-015
2.9	4.6182e-015	1.5699e-015	6.2628e-015
3	6.6105e-015	2.2216e-015	8.8584e-015
3.1	9.4428e-015	3.1379e-015	1.2505e-014
3.2	1.346e-014	4.4233e-015	1.7615e-014
3.3	1.9144e-014	6.2227e-015	2.476e-014
3.4	2.7167e-014	8.736e-015	3.4726e-014
3.5	3.8461e-014	1.2238e-014	4.8592e-014
3.6	5.4318e-014	1.7107e-014	6.7834e-014
3.7	7.6524e-014	2.3861e-014	9.4465e-014
3.8	1.0753e-013	3.3206e-014	1.3122e-013
3.9	1.5071e-013	4.6106e-014	1.8181e-013
4	2.1066e-013	6.3872e-014	2.5123e-013
4.1	2.9367e-013	8.8278e-014	3.4622e-013
4.2	4.0824e-013	1.2173e-013	4.7579e-013
4.3	5.6592e-013	1.6746e-013	6.5197e-013
4.4	7.8224e-013	2.2984e-013	8.9077e-013
4.5	1.0781e-012	3.147e-013	1.2133e-012
4.6	1.4814e-012	4.2989e-013	1.6475e-012
4.7	2.0294e-012	5.8584e-013	2.2297e-012
4.8	2.7713e-012	7.9644e-013	3.0076e-012
4.9	3.7723e-012	1.0801e-012	4.0425e-012
5	5.1178e-012	1.4612e-012	5.4137e-012

5. CONCLUSION

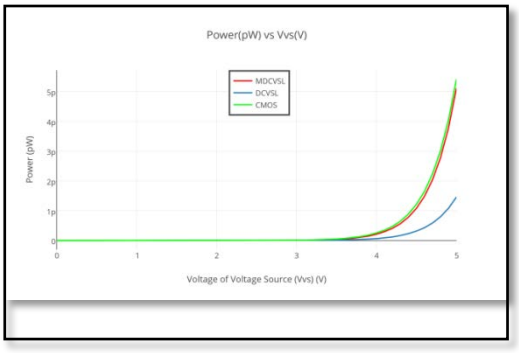

Fig 5.1. Power vs Vvs (Supply Votlage) of the three logic styles [6].

We can infer from the data shown in Figures 5.1 & 5.2 that DCVSL style emerged as the most power efficient style in either case.

When supply voltage Vvs is varied from 0 to 5 V; there is a gradual increase in the power consumption of XOR in every structure but DCVSL being the one having the minimum (i.e. 1.4612e-012) and CMOS having the maximum (5.4137e-012).

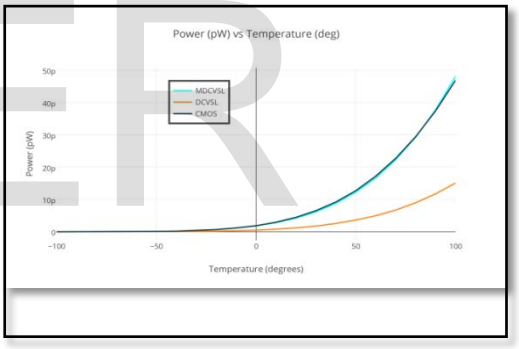

Fig 5.2. Power vs Temperature of the three logic styles [6].

Similarly, when the temperature is increased over a range of -100 to 100 Degrees, DCVSL shows minimum power consumption (i.e. 1.512e-011). Hence, DCVSL is suitable for low power consumption applications. So, we conclude that XOR gate being widely used in sequence detection, parity check, PRN generators etc, can be made power efficient using DCVSL logic style.

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